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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,961	02/06/2004	Chia-Te Wu	021653-003500US	7323

20350 7590 11/17/2004

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,961	WU ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: reference numeral 100 as shown in figure 1 and reference numeral 603 as shown in figure 6. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because figure 7 is so dark that the features shown therein cannot be ascertained. The large black area in figure 7 render it impossible to tell where most of the reference numerals are pointing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The disclosure is objected to because of the following informalities: Page 4 line 9 refers to both the substrate and the surface region using reference numeral 101. Also page 5 lines 20-21 recites "a substrate 401 including a surface region 400" while figure 4 shows 401 as pointing to the surface and 400 as being in the substrate.

Appropriate correction is required.

Claim Objections

6. Claims 11 and 12 objected to because of the following informalities: Claim 1 lines 4-5 recite "a floating gate floating gate," it appears that the second recitation of floating gate should be removed. Claim 11 line 10 should recite "including the stripe portion" and line 15 should recite 'the stripe portion traversing through". Claim 12 line 1 should recite "dielectric layer". Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 1 recites the limitation "the substrate region" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 11 recites the limitation "the substrate region" in line 4. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 17 recites the limitation "the stripe configuration" in line 1. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 20 recites the limitation "the stripe configuration" in 1. There is insufficient antecedent basis for this limitation in the claim.

12. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "a control gate overlying the floating gate overlying the insulating layer" in lines 7-8. The insulating layer has previously been claimed as being formed overlying the floating gate. Thus, this limitation is indefinite as it is unclear how the floating gate can be formed overlying the insulating layer when the insulating layer is formed overlying the floating gate.

Claim 1 recites "a portion of the gate dielectric layer" in line 9 and "the portion of the gate dielectric layer" in line 10. A "portion of the gate dielectric layer" has previously been claimed in line 4. Thus it is indefinite as to whether the limitations on lines 9 and 10 are claiming another (second or third) portion of the gate dielectric layer or whether the limitations of lines 9 and 10 are claiming the same (first) portion previously claimed.

Claim 11 recites "a control gate overlying the floating gate overlying the insulating layer" in lines 12-13. The insulating layer has previously been claimed as being formed

overlying the floating gate. Thus, this limitation is indefinite as it is unclear how the floating gate can be formed overlying the insulating layer when the insulating layer is formed overlying the floating gate.

Claims 9 and 19 recite "a cell region, the cell region" in line 2. A first cell region has previously been claims in claims 1 and 11 respectively (from which 9 and 19 depend). Thus, it is indefinite as to whether claims 9 and 19 are claiming the same cell region (first cell region) previously claimed or whether claims 9 and 19 are claiming another cell region.

Claims 2-10 and 12-20 are rejected in the same manner as claims 1 and 11, respectively, as they depend from 1 and 11 and contain all the limitations from the claim which they depend.

Claims 5 and 15 are further indefinite as it is unclear how a "design width" limits the final product. Claims 5 and 15 both recite the floating gate having a design width of 1.5 microns. It is unclear as to whether the "design width" is the actual width of the final product or a width used in designing the device, designing a mask for processing, or a width dealing with an intermediate step in the process of forming the floating gate.

Product-by-Process Limitations

13. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In*

re Avery, 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

14. Insofar as definite, the claims are rejected as follows.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1, 2, 4, 6, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Manley (U.S. Patent No. 5,404,037).

Manley disclose in figures 1-18B and on columns 1-10, an EEPROM integrated circuit structure comprising:

a substrate including a surface region (p-substrate, the surface region is considered the entire region shown in figure 15);

the surface region being provided within a first cell region (figures 16 and 17 show multiple cells of the device of figure 15, thus the surface region shown in figure 15 is considered within a first cell region as shown in figures 16 and 17);

a gate dielectric layer of first thickness overlying the surface of the substrate (labeled 13 in figure 14; not labeled in figure 15 but the gate dielectric is still under the poly 1 floating gate and is also under the poly 2 select gate, see column 6 lines 16-22);

a select gate overlying a first portion of the gate dielectric layer (poly 2 is the select gate as seen in figure 15 where it overlies a first portion of the gate dielectric);

a floating gate overlying a second portion of the gate dielectric layer and coupled to the select gate (figure 15, poly 1 is the floating gate and it overlies a second portion (thick oxide shown adjacent the left side of the tunnel oxide) of the gate dielectric, the floating gate is coupled to the select gate through the N+ region underlying the tunnel oxide);

an insulating layer overlying the floating gate (ONO as seen in figure 15);

a control gate overlying the floating gate and the insulating layer and coupled to the floating gate (poly2 is the control gate which is seen over the insulating layer and floating gate, it is couple to the floating gate through the insulating layer, figure 15);

a tunnel window provided in a stripe configuration within a portion of the gate dielectric layer of a second thickness, the second thickness being less than the first thickness (the tunnel window is labeled "tunnel oxide" in figure 15 and is shown in figure

9 for example, as being in a stripe configuration 30, the tunnel window within a portion of the gate dielectric and it is seen to have a second thickness thinner than the first thickness in figure 15).

With regard to claim 2, Manley discloses the gate dielectric being a gate oxide but does not explicitly state that the gate oxide is silicon dioxide. Nonetheless, this limitation is implicitly disclosed as Manley teach forming the gate oxide by thermal oxidation of the silicon substrate which is known to produce silicon dioxide.

With regard to claim 4, the insulating layer is an ONO layer coupled between the floating gate and control gate (figure 15, column 7 lines 1-5).

With regard to claim 6, the limitation of the tunnel window being provided by a phase shift mask is a product-by-process limitation. This product-by-process limitation does not structurally distinguish over the prior art and thus the claim is anticipated by Manley.

With regard to claim 8, though not explicitly stated, it is nonetheless implicitly understood in the art of semiconductor that the substrate is a semiconductor wafer.

With regard to claim 9, the select gate, floating gate, and control gate are provided in a cell region and the cell region is provided within an isolation region (figure 16 shows field oxide layers isolating the various cells).

17. Claims 11, 12, 14, 16, 18 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hart et al. (U.S. Patent No. 5,293,331).

Hart et al. disclose an EEPROM integrated circuit structure comprising:

a substrate 10 including a surface region (figure 7; the surface region is considered to be the region between the left and right FOX1);

the surface region being provided within a first cell region (the region shown in figure 7 is considered the first cell region);

a gate dielectric layer 22 of first thickness overlying the surface of the substrate 10 (figure 7);

a plurality of stripes 24, each stripe 24 being characterized by a second thickness, the second thickness being less than the first thickness (one stripe shown in figure 7; the cell of figure 7 is repeated in the array of figure 10 which shows a plurality of stripes labeled "tunnel oxide stripe"; as seen in figure 7 the stripe 24 has a thickness less than that of gate dielectric 22);

each stripe 24 having a predetermined width and a predetermined length (each stripe has a width and length, no patentable weight is given to "predetermined" as the term does not further structurally limit the length or width);

at least one of the stripe 24 includes a portion traversing a portion of the first cell region and other cell regions (as seen in figure 10, tunnel oxide stripe extends through and across cell A and C);

a floating gate 26 overlying a portion of the gate dielectric layer 22, the portion of the gate dielectric including the stripe portion 24 traversing through the portion of the gate dielectric layer (the floating gate 26 overlies the portion of gate dielectric 22 where the stripe 24 traverses through it; figure 7);

an insulating layer 28 overlying the floating gate (figure 7);

a control gate 30 overlying the floating gate 26 and the insulating layer 28 and coupled to the floating gate (figure 7, the control gate 30 is coupled to the floating gate 26 through the insulating layer 28); and

wherein the stripe portion 24 traversing through the portion of the first cell region includes a tunnel window for a memory device (the crossing of the floating gate 26 and the stripe 24 is the tunnel window, the device is a memory device; figure 7).

Claim 11 recites various process steps such as "forming" and "patterning." Since claim 11 is directed towards a product (the preamble recites "the structure comprising") these limitations are product-by-process limitations. The structures resulting from these limitations have been treated above. The specific processes claimed do not structurally distinguish over the device of Hart et al.

With regard to claim 12, Hart et al. disclose the gate dielectric being a gate oxide but does not explicitly state that the gate oxide is silicon dioxide. Nonetheless, this limitation is implicitly disclosed as Hart et al. teach forming the gate oxide by thermal oxidation of the silicon substrate which is known to produce silicon dioxide.

With regard to claim 14, the insulating layer 28 is an ONO layer coupled between the floating gate and the control gate (figure 7; column 6 lines 38-40).

With regard to claim 16, the limitation of the tunnel window being provided by a phase shift mask is a product-by-process limitation. This product-by-process limitation does not structurally distinguish over the prior art and thus the claim is anticipated by Hart et al.

With regard to claim 18, though not explicitly stated, it is nonetheless implicitly understood in the art of semiconductor that the substrate is a semiconductor wafer.

With regard to claim 19, the floating gate and control gate are provided within a cell region which is provided within an isolation region (figures 7 and 8 show the floating gate and control gate in the cell region between isolation regions FOX1).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manley (U.S. Patent No. 5,404,037) as applied to claims 1, 2, 4, 6, 8 and 9 above.

With regard to claim 3, Manley does not explicitly teach the width of the tunnel window.

With regard to claim 5, the "design width" is being interpreted to be the final width of the floating gate in the final product. Manley does not explicitly teach the floating gate having a width of 1.5 microns.

Nonetheless, these claimed dimensions are considered obvious to one of ordinary skill in the art in view of Manley. One of ordinary skill in the art is motivated to form device features as small as possible to allow as many devices as possible to be formed simultaneously on a single wafer, thus saving of processing costs per device. It

would have been obvious to form the tunnel window to a width of less than 0.25 microns to allow the device to be formed as small as possible. It would have been obvious to form the floating gate to a width of 1.5 microns to form the device to a minimal size to allow for greater packing of devices on the chip.

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

20. Claims 13, 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al. (U.S. Patent No. 5,293,331) as applied to claims 11, 12, 14, 16, 18 and 19 above.

With regard to claim 13, Hart et al. do not explicitly teach the width of the tunnel window.

With regard to claim 15, the "design width" is being interpreted to be the final width of the floating gate in the final product. Hart et al. do not explicitly teach the floating gate having a width of 1.5 microns.

Nonetheless, these claimed dimensions are considered obvious to one of ordinary skill in the art in view of Hart et al. One of ordinary skill in the art is motivated to form device features as small as possible to allow as many devices as possible to be formed simultaneously on a single wafer, thus saving of processing costs per device. It would have been obvious to form the tunnel window to a width of less than 0.25 microns to allow the device to be formed as small as possible. It would have been obvious to form the floating gate to a width of 1.5 microns to form the device to a minimal size to allow for greater packing of devices on the chip.

These claims are prima facie obvious without showing that the claimed ranges achieve unexpected results relative to the prior art range. In re Woodruff, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also In re Huang, 40 USPQ2d 1685, 1688(Fed. Cir. 1996)(claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also In re Boesch, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and In re Aller, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

With regard to claim 20, Hart et al. teach an array of their EEPROM cells. For example, figure 10 shows four cells in a 2x2 array. The stripe configuration of Hart et al. runs through the first cell (A) to a second cell (C). However, Hart et al. do not explicitly teach the stripe running through other cell regions numbered from 2 through N, where N is an integer greater than 2 (i.e. Hart et al. figure 10 only shows the tunnel oxide stripe running through 2 cells A and C, but the claim requires a minimum of three cells). Official Notice is taken that it would have been obvious to one of ordinary skill in the art at the time of the invention to form the array of Hart et al. figure 10 to a size much greater than 2x2. It would have been obvious to form the array to a size greater than 2x2 (i.e. including at least 3 cells in each row and column such that each tunnel oxide stripe runs through at least 3 cells) to allow the array to hold a greater number of bits of data. It is well known in the art to form memory chips to hold megabits or more of information so that greater storage can be achieved in each chip. Thus, it would have been obvious to one of ordinary skill in the art to form the tunnel oxide stripe of Hart et al. running across many cells.

21. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al. as applied to claims 11, 12, 14, 16, 18 and 19 above, and further in view of D'Arrigo et al. (U.S. Patent No. 5,168,335).

Hart et al. teaches in figures 8 and 10 the stripe configuration running through a plurality of cells (cells A and C for example) and teaches adjacent cells in the word line direction being separated by a field oxide region. However, Hart et al. do not teach

each cell the stripe runs through being separated from the other cells the same stripe runs through.

D'Arrigo et al. teach an EEPROM in figures 7 and 8, for example. D'Arrigo et al. teach a device having a floating gate 46a,46b and a control gate 62 with a tunnel window 40a in the gate insulating layer beneath the floating gate. D'Arrigo et al. teach an array of such devices in figure 8 and teaches that each cell is isolated from all adjacent cells by field oxide regions 24, 84 and 86.

Hart et al. and D'Arrigo et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to isolate each cell by a field oxide region. The motivation for doing so is to provide proper deice isolation so that each cell can be addressed, read, or written singly and without causing substrate conduction that could effect an adjacent cell. Therefore, it would have been obvious to combine Hart et al. with D'Arrigo et al. to obtain the invention of claims 17.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yaron et al. (U.S. Patent No. 4477825), Radjy et al. (U.S. Patent No. 5005155), Chang et al. (U.S. Patent No. 5273923), JP 4-116985 A.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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